REMARKS

The above-referenced patent application has been reviewed in light of the Final Office Action, dated March 7, 2001. Claims 1-11 and 21-26 are rejected under 35 USC 103(a) as being unpatentable over Tran et al. (hereinafter "Tran") in view of Sato. Claims 27-43 are allowed. Reconsideration of the above-referenced patent application in view of the foregoing amendment and the following remarks is respectfully requested.

Claims 1-12 and 21-26 are now pending the above-referenced patent application. Claims 13-20 have been withdrawn from consideration and will be pursued in a separate continuation patent application. No prosecution history estoppel therefore applies with respect to the cancellation of these claims. Likewise, claim 12, previously cancelled, has been replaced in the present application as claim 44, and claims 1 and 21 have been amended to remove the limitations that are now present in claim 44. Therefore, no prosecution history estoppel results from the previous cancellation of claim 12.

The Examiner has rejected claims 1-11 and 21-26 under 35 USC 103(a) as being unpatentable over Tran in view of Sato. This rejection is respectfully traversed.

It is noted that claims 1 and 21 have been broadened. In particular, the limitations of original claim 12 that were added to these claims have been removed. New claim 44, which has been added, now contains these limitations and depends from claim 1. As previously indicated, no prosecution history estoppel results from the previous cancellation of claim 12.

It has previously been argued that claims 1 and 21 distinguish from the cited patents by reciting **diffusion regions having partially overlying polysilicon landing sites, at least one forming N-type and P-typ transistors**. As previously argued, Tran is disadvantageous because it would require additional design complexity. **For example, Tran would require additional layers of metallization to connect N-type and P-type transistors.**

In the Final Office Action, the Examiner has attempted to combine Tran and Sato to respond to this argument. In this regard, the Examiner states: "Sato discloses in figure 9 that one gate can be formed on both N-type and P-type transistors. Therefore, it would have been obvious to one of ordinary skill in the art to form the polysilicon gate of Tran on both N-type and P-type transistors as taught by Sato." It is respectfully asserted that this is insufficient to overcome Applicant's argument for a variety of reasons.

First, even assuming for the sake of argument that Tran and Sato could be combined, as the Examiner asserts, although Applicant argues below that they may not, nonetheless, the combination would fail to produce the invention as recited in claim 1, as amended.

The Examiner is attempting to use Sato to provide the aspect of claim 1 that Tran is missing; however, neither Tran nor Sato, either individually or in combination, provides a polysilicon landing site overlying diffusion regions to form both N-type and P-type transistors. **In particular, the Examiner has pointed to figure 9 of Sato, as indicated above. However, figure 9 of Sato is not relevant at all. To the contrary, figure 9 is a circuit diagram of a RAM cell and does not illustrate the layout to fabricate a cell using polysilicon landings and diffusion regions.** Therefore, even if one of ordinary skill in the art were to combine Tran and Sato, it would fail to produce the invention as recited in claim 1. **At best, the combination of Tran and Sato, even assuming the combination is pr per, which is disputed below, shows polysilicon landings overlying either N-type or P-typ diffusion regions, not overlying diffusion regions to form both N-type and P-type transistors.** As previously indicated, one advantage of the approach recited in claim 1 is that design complexity is reduced. For example, additional layers of metallization to connect the N-type and P-type transistors are avoided. However, one of ordinary skill in the art would not be able to produce this result from the asserted combination.

Furthermore, Tran and Sato is not a proper combination because one of ordinary skill in the art would not be motivated to make it. As is well-established Federal Circuit law, there must be a motivation shown in the prior art for the combination. Here, such a motivation has not been demonstrated. **In particular, as pr vious indicated, th figur p int d to by th Examin r, figur**

9, is n t a gat array archit ctur lay ut for a c ll, but, inst ad a circuit diagram. Th refor , th figur is not at all r l vant to polysilicon landings. Furthermor , th r is no t aching, r v n sugg stion, in ither Tran or Sat , that, by employing a polysilic n landing ov r both P-typ and N-type diffusion regions in a gate array architecture, additional layers of metallization may b avoided. Therefore, the required motivation for the combination has not been provided.

It is, therefore, respectfully asserted that the rejected claims, 1-12 and 21-26, patentably distinguish from the cited patents. It is, therefore, respectfully requested that the rejection of these claims be withdrawn.

CONCLUSION

In view of the foregoing, it is respectfully asserted that the claims pending in this application, as amended, are in condition for allowance. If the Examiner has any questions, he is invited to contact the undersigned at (503) 264-0967. Reconsideration of this patent application and early allowance of these claims is respectfully requested.

Respectfully submitted,

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MARKED VERSION OF THE CLAIMS TO SHOW CHANGES

(amended three times)1. An integrated circuit comprising: a gate array architecture;

said gate array architecture including a semiconductor substrate having a plurality of N-type diffusion regions and P-type diffusion regions; said diffusion regions having partially overlying polysilicon landing sites, at least one forming both N-type and P-type transistors;

wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P-type transistors[;

successive rows of small diffusion regions are followed by successive rows of regular-siz d diffusion regions; and

immediately successive rows within similarly-sized regions have opposite polarity].

(amended three times)21. An article comprising: a storage medium, said storage medium having instructions stored thereon, said instructions, when executed, resulting in the capability to design the layout of an integrated circuit chip for fabrication, the integrated circuit chip including a gate array architecture;

the gate array architecture including a semiconductor substrate having a plurality of N-type diffusion regions and P-type diffusion regions; said diffusion regions having partially overlying polysilicon landing sites, at least one forming both N-type and P-type transistors;

wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P-type transistors[;

succ ssiv rows of small diffusion regions ar f llow d by succ ssiv rows of r gular-siz d diffusion regi ns; and

imm diately succ ssiv rows within similarly-siz d regions hav opposit polarity].

New claim:

44. <u>The integrat d circuit of claim 1, wh rein successiv r ws of small diffusion regions ar f llowed by successive rows of regular-sized diffusion regions;</u>

<u>wherein immediately successive rows within similarly-sized diffusion regions have pposite polarity.</u>

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